REMARKS

Please reconsider the present application in view of the above amendments and following remarks. Applicant thanks the Examiner for carefully considering this application.

Disposition of the Claims

Claims 4, 16, and 27 were pending in this application. By way of this reply, claims 28-33 were added. Therefore, claims 4, 16, 27, and 28-33 are currently pending in this application. Claims 4, 16, and 27 are independent. Claims 28-33 depend, directly or indirectly, from the independent claims.

Claim Amendments

By way of this reply, claims 4, 16, and 27 have been amended, and claims 28-33 have been added. Claim 4 has been amended to recite, in part, "said presuming comprises: deleting analysis points corresponding to the test pattern sequence where the transient power supply current does not show abnormality from analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality; and presuming a remaining analysis point out of the analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality to be a fault location." Claims 16 and 27 have been amended to recite substantially similar limitations. Support for these amendments may be found throughout the specification, *e.g.*, in paragraph [0022] of the published specification. Claims 16 and 27 have also been amended to change "for" to "configured to," as suggested by the Examiner. New claims 28-30 recite that the semiconductor IC is a CMOS IC. Support for this limitation may be found throughout the specification, *e.g.*, paragraph [0086]. Finally, new claims 31-33 recite additional features of the time integral of the

transient power supply current. Support for this limitation may be found throughout the specification, *e.g.,* paragraph [0141]. No new matter has been added by way of these amendments.

Claim Objection

Claims 16 and 27 are objected to because the claims recite the term "for" as opposed to "configured to" (*see* page 2 of the instant Office Action). Without acquiescing to the propriety of this objection, amendments have been made as suggested by the Examiner to expedite prosecution. Accordingly, withdrawal of this objection is respectfully requested.

Claim Rejections under 35 U.S.C. § 103(a)

Claims 4, 16, and 27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,043,672 ("Sugasawara"). As noted above, claims 4, 16, and 27 have been amended. To the extent that this rejection may still apply to amended claims 4, 16, and 27 and new claims 28-33, the rejection is respectfully traversed.

MPEP § 706.02(j) provides, "to support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Further, in *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727 (2007), the Supreme Court noted that the analysis supporting a rejection under 35 U.S.C. § 103 should be made explicit. Hence, the key to supporting any rejection under § 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious (*see* MPEP §§ 2141, 2142).

In response to Applicant's arguments filed October 31, 2008, the Examiner made the following comments on page 10 of the instant Office Action:

> [A]lthough Sugasawara may not explicitly recite "transient current" and recites "quiescent current," it is reasonable to expect one of ordinary skill in the art at the time of the applicants' invention to utilize different defect detection methodologies that are common (i.e., "transient" and "quiescent") particularly if the steps and functionality are similar.

Applicant respectfully disagrees with the Examiner's assumption that transient current and quiescent current are obvious substitutes. The fact that one method may be an alternative to another does not necessarily support a conclusion of obviousness. Specifically, transient current testing and quiescent current testing are two separate defect detection methods, requiring different analyses, experiments, and applications. For example, as is clear from the literature provided by the Examiner, transient current testing represents a different and significantly faster method for defect detection compared to the conventional defect detection testing using quiescent current (*see* page 1 of Manoj Sachdev, Peter Janssen, & Victor Zieren, *Defect Detection with Transient Current Testing and its Potential for Deep Sub-micron CMOS ICs*). Therefore, contrary to the Examiner's arguments, the claimed invention is not merely a simple substitution of a known element disclosed in Sugasawara.

Applicant respectfully asserts that the Examiner has simply demonstrated that quiescent current testing is one alternative for transient current testing, and has not clearly articulated the reason(s) why or how the transient current testing of the claimed invention would have been obvious in light of Sugasawara's quiescent current testing (*see* MPEP §§ 2141, 2142).

Hence, Applicant respectfully notes that the Examiner's arguments do not support a prima facie case of obviousness under 35 U.S.C. § 103(a).

However, Applicant appreciates the Examiner for offering suggestions in which Applicant could distinguish the claims from the prior art of record (*see* page 11 of the instant Office Action). Although Applicant respectfully disagrees with the Examiner's grounds for rejection, in the interest of expediting prosecution, Applicant has amended the claims in accordance with the Examiner's suggestions.

Specifically, independent claims 4, 16, and 27 have been amended to recite, in part, "deleting analysis points corresponding to the test pattern sequence where the transient power supply current does not show abnormality from analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality; and presuming a remaining analysis point out of the analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality to be a fault location." The other suggested features were incorporated in new claims 28-33. Specifically, new claims 28-31 recite, "wherein the semiconductor IC is a CMOS IC," and new claims 31-33 recite, "wherein the time integral of said transient power supply current is a sum of integrals of transient currents that flow in logic gates of the CMOS IC." As the Examiner noted, Sugasawara does not teach or suggest at least these limitations.

In view of the above, amended independent claims 4, 16, and 27 and new claims 28-33 are patentable over Suagasawara. Accordingly, withdrawal of this rejection is respectfully requested.

Double patenting Issues

On page 11 of the instant Office Action, the Examiner noted that "U.S. Patent No.'s US-6828815-B2 and US-6801049-B2 may create double patenting issues (that may be resolvable with a Terminal Disclaimer) with respect to the pending application, however, the examiner has not issued a double patenting rejection at this point in time since the applicants' claims appear to be directed to additional aspects not claimed but found with their Specification."

MPEP § 804 makes clear that a double patenting rejection must rely on a comparison with the *claims* in an issued or to be issued patent (whereas an anticipation or obviousness rejection based on the same patent(s) under 35 U.S.C. §§ 102 or 103 relies on a comparison with *everything that is disclosed* in the same issued or to be issued patent). As explained above, the claims of the present application have been amended to add additional aspects as suggested by the Examiner. Amended claims 4, 16, and 27 and new claims 28-33 do not correspond to and are not obvious over the claims of the aforementioned patent. Accordingly, Applicant respectfully asserts that the claims of the present application do not raise any double patenting issues.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591, Reference No. 02008/071003.

Dated: March 10, 2009

Respectfully submitted,

By: _____

Thomas K. Scherer
Registration No.: 45,079
OSHA · LIANG LLP
909 Fannin Street, Suite 3500
Houston, Texas 77010
(713) 228-8600
(713) 228-8778 (Fax)
Attorney for Applicant